

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.: 09/632,543
Appellant: Talluri et al
Filed: August 4, 2000
TC/AU: 2612
Examiner: Nguyen

Confirmation No.: 1760

Docket: T1-28919
Cust.No.: 23494

SUBSTITUTE APPEAL BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed 09/07/2006, appellant hereby submits the attached sheets which contain the Rule 41.37 items of appellant's substitute Appeal Brief. The fee for filing a brief in support of the appeal has previously been paid. The Director is hereby authorized to charge any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Pursuant to MPEP 1205.02, for each claim in the case appellant states the status as follows:

Claim 1: rejected

Claim 2: cancelled

Claim 3: rejected

Claim 4: rejected

Claim 5: rejected

Claim 6: rejected

Pursuant to MPEP 1205.02, appellant identifies each claim on appeal as follows

Claim 1: on appeal

Claim 3: on appeal

Claim 4: on appeal

Claim 5: on appeal

Claim 6: on appeal

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The independent claims on appeal consist of integrated circuit claim 1, integrated circuit claim 3, and integrated circuit claim 4.

The subject matter of claim 1 is an integrated circuit for a digital still camera with a first programmable processor programmed to run control functions (FIG.1b 130; application page 4, lines 22-25; page 5, lines 16-17), the first

processor coupled to a user interface (FIG.1b 140; application page 5, lines 22-23), to a controller for memory (FIG.1b 110; application page 4, lines 26-27), and to a controller for image acquisition (FIG.1b 102; application page 6, lines 28-29); a second programmable processor programmed to run image processing and compression functions (FIG. 1b 122; application page 4, line 18), the second processor coupled to said first processor (FIG.1b bus; application page 7, line 11); and a third processor coupled to said second processor (FIG.1b 124; application page 4, lines 14-21), the third processor including at least four parallel multiply and accumulate units (FIG. 19; application page 67, lines 4-5).

The subject matter of claim 3 is an integrated circuit for a digital still camera, with a first programmable processor programmed to run control functions (FIG.1b 130; application page 4, lines 22-25; page 5, lines 16-17), said first processor coupled to a user interface (FIG.1b 140; application page 5, lines 22-23), a controller for memory (FIG.1b 110; application page 4, lines 26-27), and a controller for image acquisition (FIG.1b 102; application page 6, lines 28-29); a second programmable processor programmed to run image processing and compression functions (FIG. 1b 122; application page 4, line 18), said second processor coupled to said first processor (FIG.1b bus; application page 7, line 11); and an image compression unit separate from said second processor (FIG.1b 108; application page 4, line 9), said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory (FIGs. 5-6; application page 7, lines 17-24).

The subject matter of claim 4 is an integrated circuit for a digital still camera, with a first programmable processor programmed to run control functions (FIG.1b 130; application page 4, lines 22-25; page 5, lines 16-17), said first processor coupled to a user interface (FIG.1b 140; application page 5, lines 22-23), a controller for memory (FIG.1b 110; application page 4, lines 26-27), and a controller for image acquisition (FIG.1b 102; application page 6, lines 28-29); a second programmable processor programmed to run image processing and compression functions (FIG. 1b 122; application page 4, line 18), said

second processor coupled to said first processor (FIG.1b bus; application page 7, line 11); and a digital image processing unit separate from said first and second processors (FIG.1b 104; application page 4, line 7), said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor (FIG.2; application page 6, lines 14-27).

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

- (1) Claim 1 was rejected under 35 USC § 102 as anticipated by Duncan.
- (2) Claim 4 was rejected under 35 USC § 102 as anticipated by Fukuoka.
- (3) Claim 3 was rejected under 35 USC § 103 as unpatentable over Safai in view of Mizutani.

(4) Claim 5 was rejected under 35 USC § 103 as unpatentable over Duncan in view of Fukuoka.

(5) Claim 6 was rejected under 35 USC § 103 as unpatentable over Duncan in view of Safai and Mizutani.

Rule 41.37(c)(1)(vii) Arguments

(1) Claim 1 was rejected as anticipated by Duncan; the Examiner cited the multipliers 630-633 and latches 640-643 in Fig.61 as the four parallel multiply and accumulate (MAC) units required by claim 1.

Claim 1: Appellants reply that the cited multipliers plus latches of Duncan do not suggest the four parallel multiply and accumulate units because there is no accumulation for each multiplier. Rather, the outputs of the four multipliers are stored in the four latches, but the contents of the four latches are added together (by adders 644-645, latches 646-647, and adder 648) prior to any accumulation by single accumulator 680 (see Duncan column 15, lines 25-28). Thus Duncan does not suggest claim 1.

(2) Claim 4 was rejected as anticipated by Fukuoka; the Examiner cited Fukuoka Fig.1 CPU 11 for the first processor, compression circuit 7 for the second processor, and DSP 6 for the image processor.

Claim 4: Appellants reply that claim 4 requires a programmable second processor for image compression; whereas, Fukuoka only describes CPU 11 as doing various tasks (i.e., programmable) but does not suggest any programmability of compression circuit 7.

(3) Claim 3 was rejected as unpatentable over Safai in view of Mizutani; the Examiner cited Safai processors 312 and 310 of Fig.3 for the first and second processors of the claim and cited Mizutani JPEG unit 29 as the image compression unit.

Claim 3: Appellants reply that claim 3 requires first and second processors plus a separate image compression unit; whereas Safai has image compression already in image processor 310 (see Safai Fig.4), and there is no suggestion to include another unit for image compression. Furthermore, claim 3 requires the separate image compression unit be able to act on the acquired image; in contrast, Mizutani Fig.2 shows JPEG unit 29 applied after input processing 21 and memory controller 22 and thus not acting on the acquired image. Indeed, Mizutani Fig.4 explicitly shows input processing 21 performs RGB → YCbCr color space conversion. (Application Fig.1b shows burst mode compression/decompression unit 108 directly connected to the CCD controller to get the acquired image, whereas DSP subsystem 120 gets an image from memory.)

(4) Claim 5 was rejected as unpatentable over Duncan in view of Fukuoka.

Claim 5: Appellants rely upon the patentability of parent claim 1.

(5) Claim 6 was rejected as unpatentable over the Duncan in view of Safai and Mizutani.

Claim 6: Appellants rely upon the patentability of parent claim 1.

Rule 41.37(c)(1)(viii) Claims appendix

1. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a third processor coupled to said second processor, said third processor including at least four parallel multiply and accumulate units.

3. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) an image compression unit separate from said second processor, said compression unit arranged to compress acquired images for storage in a memory and to decompress said compressed acquired images in said memory for restorage in said memory.

4. An integrated circuit for a digital still camera, comprising:

(a) a first programmable processor programmed to run control functions, said first processor coupled to a user interface, a controller for memory, and a controller for image acquisition;

(b) a second programmable processor programmed to run image processing and compression functions, said second processor coupled to said first processor; and

(c) a digital image processing unit separate from said first and second processors, said image processing unit arranged for real-time image sequence (video) processing, said image processing unit controlled in real-time by said first processor

5. The integrated circuit of claim 1, further comprising:

(a) an audio input coupled to said second processor, said second processor programmed to decode audio and said first processor programmed to output said decoded audio.

6. The integrated circuit of claim 1, further comprising:

(a) camera peripherals including IfSA, USB, NTSC/PAL encoder, and compact flash/smart media interface.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none